REMARKS

DRAWINGS

Since several drawings of a two-winding transformer are already included in the drawings (Figs. 3 and 4), applicants suggest simply inserting at line 4 of paragraph 0078 after "transformers" the following: (like the ones shown in Figs. 3 and 4). If such an approach is acceptable to the examiner, an appropriate amendment will be made in responding to the next office action.

35 U.S.C. §112, FIRST PARAGRAPH, REJECTIONS

Claims 6-17

There are no specific combinations of assignments between the modulation technique and the specific associated data.

What the specification does is teach a person skilled in the art how to generate (1) waveforms associated with a phase shift keying and the data to be transmitted (see paragraph 0072), (2) waveforms associated with frequency shift keying and the data to be transmitted (see paragraph 0073), and (3) waveforms that simultaneously use phase shift keying and frequency shift keying to transmit information (see paragraph 0074). The clock signals referred to in these paragraphs and their frequencies are defined in paragraphs 0060 and 0061.

Claims 20-24

Applicants have shown possession of the claimed invention by describing a generic correlation detection system for identifying a received bit.

The technology which provides the basis of the resonance-tracking demodulator 15 in the reader (Fig. 1) is described in numerous textbooks and handbooks. The means for identifying a received bit (Claim 19) is a correlation detector system consisting of balanced mixers 81 and 82 and sampled integrators 83 and 84 in Fig. 6 and the corresponding devices in Fig. 7. The balanced mixers provide the means for multiplying an amplitude-demodulated received signal with zero-phase, zero-average square wave C_{cm0} or C_{cm1} reference signals. Specification, paragraphs 0058, 0059. The sampled integrators provide the integration means required in a correlation detector system.

A person skilled in the art would recognize that weighted integrations (as in claims 20-22) might be desirable for the purpose of suppressing intersymbol interference and the incorporation of such weights in the C_{cm0} or C_{cm1} reference signals is easily accomplished when the signals are generated by the VCO/CGC 13 (Fig. 1). This process, often referred to as "windowing", is also described in numerous textbooks and handbooks (see Attachment I, *Electronics Engineers' Handbook, Fourth Edition*, McGraw-Hill, New York, N.Y., 1997).

The examiner points out that the specification does not describe the specific weighted integrations claimed. Since specific weighting functions have been described, analyzed, and discussed extensively in the literature (see Attachment II, *The Industrial Electronics Handbook, IEEE Press*, CRC Press LLC, Boca Raton, FL, 1997), it should not be necessary to repeat this material in the specification.

but you claim it

Claim 40

The two-winding transformer associated with each transistor is described in paragraph 0078 of the specification.

35 U.S.C. §112, SECOND PARAGRAPH, REJECTIONS

Claims 32-35

The antecedent basis for the term "data" (transmitted by the tag) appearing on line 6 is the term "data" appearing on line 1. "Sequence" in the term "data sequence" indicates that the "data" has an ordered arrival at the reader and is thus an inherent property of the data transmitted by the tag and needs no antecedent basis. *See* MPEP § 2173.05(e).

The antecedent basis for the term "tag data" on line 9 is provided by "a tag data group of T bits" on line 3. The fact that "tag data" is defined in the preamble as being a group of T bits does not make the use of the term "tag data" by itself indefinite. *See* MPEP § 2173.05(e).

The antecedent basis for the term "data group" on line 4 is also provided by "a tag data group of T bits" on line 3. The use of the abbreviated term "data group" does not make the limitation in which it appears indefinite since there is no possibility of interpreting "data group" as being either the "sync sequence" or the "error-detecting group".

Claim 33

The "preamble" is defined in claim 32 as being a sync sequence of S bits. A "message" is defined as "comprising a preamble . . . , a tag data group of T bits, and an error-detecting group of E bits." The preamble contains no elements other than the "sync sequence".

35 U.S.C. §102(b) REJECTIONS (Anticipation by Waraksa et al.)

Claim 32

Claim 32 reads as follows:

32. A reader for use with a tag that communicates data to the reader by repeating a message a plurality of times, the message comprising ***[1] a preamble consisting of a sync***

sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits, [2] the data group and the error-detecting group possibly including false-sync sequences, the reader comprising:

[3] a means for receiving the data sequence transmitted by the tag;

[4] a means for detecting each sync sequence in the received data sequence;

[5] a means for identifying the preamble;

[6] a means for extracting the tag data from the received data sequence utilizing the identification of the preamble.

The limitations shown in bold face are not disclosed by Waraksa et al..

Limitation [1]

The claim-32 limitations are expressed in terms of data bits, a message comprising an S-bit sync sequence, a T-bit tag data group, and an E-bit error-correcting group. Waraksa et al. does not transmit a data bit sequence as a sync sequence. Waraksa et al. transmits what he calls a "sync pattern" made up of "transition bits" (Waraksa et al., col. 6, table) which Waraksa et al. identifies as an "illegal pattern for Miller encoding" (Waraksa et al., col. 7, line2) since it cannot be decoded into a sequence of data bits. Thus, Waraksa et al. does not disclose applicants' sync sequence consisting of an arbitrary sequence of data bits.

Limitation [2]

Since Waraksa et al.'s "sync pattern" cannot occur in any sequence of data bits, Waraksa et al. does not disclose applicants' limitation which permits ***the data group and the error-detecting group possibly including false-sync sequences***. Waraksa et al., col. 7, lines 2-4.

Limitation [3]

Applicants require a means for receiving the data sequence transmitted by the tag which includes the sync data bits. Waraksa et al.'s receiver/controller is unable to obtain sync data bits

from Waraksa et al.'s "sync pattern" since there are no data bits that correspond to Waraksa et al.'s "sync pattern". Thus, Waraksa et al. also does not disclose Limitation [3].

Limitation [4]

N.C.

Since Waraksa et al. does not utilize sync sequences made up of ordinary data bits, Waraksa et al. obviously does not disclose any means for detecting such sync sequences in the received data sequence.

Limitation [5]

Since there is no possibility that Waraksa et al.'s "sync pattern" could be confused with any sequence of data bits, Waraksa et al. does not disclose any means for examining all of the data bits in Waraksa et al.'s message and identifying an S-bit sync sequence that appears therein.

Limitation [6]

Waraksa et al. do not have the problem of determining where among the data bits transmitted is the tag data and thus do not disclose a means for accomplishing this task.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. UnionOil Co. of California,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). (Cited in MPEP § 2131.)

Waraksa et al. does not describe each and every element of claim 32 and therefore did not anticipate applicants' claim-32 invention.

Claim 32 is written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its *en banc* decision *In re Donaldson Co.*, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means**

or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ."

MPEP § 2181.

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing Limitations [3], [4], [5], and [6]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim 32 invention.

Claim 33

Claim 33 reads as follows:

33. The reader of claim 32 wherein the preamble identifying means comprises:

a means for detecting errors in the T + E bits following each detected sync sequence assuming that the sequence in question is the preamble, the presence of errors indicating that the sync sequence in question is a false-sync sequence, the absence of errors indicating that the sequence is, in fact, the preamble.

Waraksa et al. do not disclose using the detection of errors in the data group and the error-detecting group as the means for recognizing a false-sync sequence. Waraksa et al. have no need for recognizing a false-sync sequence since they use a special "sync pattern" which cannot appear in the regular message data.

Waraksa et al. does not describe each and every element of claim 33 and therefore did not anticipate applicants' claim-33 invention.

Claim 33 is also written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph. The comparison of the Waraksa et al. and applicants emodiments made above under the ***Claim 32*** heading also apply to claim 33. There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim-33 invention.

Claim 72

Claim 72 reads as follows:

72. A method of receiving a communication from a tag which transmits a repeating message comprising ***[1] a preamble consisting a sync sequence of S bits****, a tag data group of T bits, and an error-detecting group of E bits,* ***[2] the data group and the error-detecting group possibly including false-sync sequences****, the method comprising the steps:*

[3] receiving the data sequence transmitted by the tag;

[4] detecting each sync sequence in the received data sequence;

[5] identifying the preamble;

[6] extracting the tag data from the received data sequence utilizing the identification of the preamble.

The limitations of method claim 72 are essentially the same as those of apparatus claim 32. As discussed above under the ***Claim 32*** heading, Waraksa et al. does not disclose Limitations [1], [2], [3], [4], [5], and [6].

Waraksa et al. does not describe each and every element of claim 72 and therefore did not anticipate applicants' claim-72 invention.

Claim 72 is written in a step-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph.

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing Limitations [1], [2], [3], [4], [5], and [6]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received

data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim-72 invention.

35 U.S.C. §102(e) REJECTIONS (Anticipation by Buchele)

Claims 36 and 39

Claim 36 reads as follows:

36. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

[1] a means for coupling the capacitor(s) to the coil;

[2] a means for driving the coil through the capacitor(s) with a driving signal, *the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor;*

a means for generating at least one control signal.

Limitations [1] and [2] of claim 36 are written in means-plus-function formats and are thus subject to the requirements of 35 U.S.C. 112, sixth paragraph:

"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its *en banc* decision *In re Donaldson Co.*, 16 F.3d 1189, 29 USPQ2d 1845

(Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.

Applicants' embodiment of the claim-36 invention (Fig. 1) corresponds to driver 11 supplying a driving signal through capacitors 9 and a coupling circuit 7 to a coil 5. Details of driver 11 are shown in Fig. 8. A comparison with Buchele's Fig. 2 shows the source of the driving signals (i.e. the alternating current signal that drives the coil 190) are the transistor connections (136, 144) and (126,154) which connect directly to the coil connection points 192 and 194. The driving signal does not pass through any capacitors that are connected to the coil by means of a coupling circuit. Buchele's circuit is not an equivalent of applicants' circuit and Buchele thus did not anticipate applicants' claim-36 invention. Since claim 39 depends from claim 36, Buchele also did not anticipate applicants' claim-39 invention.

Buchele's capacitor 160 merely provides a means for conserving the energy used in driving the coil and avoiding a rapid discharge of battery 170. *See* Buchele, col. 7, lines 1-12.

Claim 37

Buchele does not disclose the limitation of claim 37 and thus did not anticipate applicants' claim-37 invention

Claim 38

Buchele does not disclose the limitations of claim 38 and thus did not anticipate applicants' claim-38 invention

Claim 40

Buchele does not disclose the limitation of claim 40 and thus did not anticipate applicants' claim-40 invention

35 U.S.C. §102(e) REJECTIONS (Anticipation by Carroll et al.)

Claim 70

Claim 70 reads as follows:

70. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to a tag in the alternating magnetic field.

Carroll et al. does not disclose the limitation in boldface. The figure cited by the examiner (Carroll et al., Fig. 4b) refers to the situation when transponder 40 has responded to an interrogation by controller 10 and controller 10 has bit-synchronized to transponder 40's transmission (Carroll et al., col. 14, line 60 - col. 15, line 67). Then (with reference to Fig. 4B), controller 10 "either reads from, or writes to, the non-volatile memory 48 of the transponder 40 by sending a command word 112. The command word 112 is transmitted in bit for bit synchronization with the configuration word 100 or any data being sent from the transponder 40 to the controller 10." Carroll et al., col. 16, lines 1-10. Synchronization block 114 are logic level zero bits and is NOT a bit-timing clock signal. Carroll et al., col. 16, lines 7-10.

Carroll et al.'s controller 10 only transmits FSK modulated data signals. Carroll et al., col. 6, lines 7-9; col. 7, lines 5-12. Carroll et al. does not embed a bit-timing clock signal in the alternating magnetic field because FSK detector 64 in transponder 40 does not require a bit-

timing signal. *See* references cited, Carroll et al., col. 12, lines 36-46.

Carroll et al. does not describe each and every element of claim 70 and therefore did not anticipate applicants' claim-70 invention.

Claim 71

Claim 71 reads as follows:

71. A method for interrogating a tag, ***[1] the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator****, the method comprising the steps:*

[2] generating a bit-timing clock signal;

[3] generating an alternating magnetic field in which the bit-timing clock signal is embedded;

[4] extracting data transmitted by the tag utilizing the bit-timing clock signal.

Carroll et al. does not disclose any of the four limitations shown in boldface.

Limitation [1]

Preamble

Carroll et al.'s transponder 40 responds to an interrogation by transmitting a sequence of bits in accordance with a bit-timing clock signal generated by transponder 40, but the bit-timing clock is not synchronized with a bit-timing clock signal originating with controller 10. Carroll et al.'s bit-timing clock in transponder 40 is obtained by dividing down the frequency of the interrogating signal. Carroll et al., col. 12, line 20 - col. 13, line 7. As discussed above under the ***Claim 70*** heading, controller 10 does not send a bit-timing clock signal to transponder 40, and transponder 40 does not require one.

Limitation [2]

Carroll et al.'s controller 10 does not generate a bit-timing signal which, as the claim preamble specifies, is the bit-timing reference for both controller 10 and transponder 40. Please see discussion under the ***Claim 70*** heading and also under the ***Limitation [1]*** heading above.

Limitation [3]

Carroll et al.'s controller 10 does not embed a bit-timing clock signal in the interrogating signal transmitted to transponder 40. Please see discussion under the ***Claim 70*** heading.

Limitation [4]

Carroll et al.'s controller 10 does not extract the data carried by the signal transmitted by transponder 40 using a bit-timing signal originating in controller 10. Carroll et al.'s controller 10 does not generate such a signal and obviously cannot use it in extracting the data sent by transponder 40.

Carroll et al. does not describe each and every element of claim 71 and therefore did not anticipate applicants' claim-71 invention.

Claim 73

Claim 73 reads as follows:

73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal;

maintaining the resonating circuit in resonance;

embedding the sequence of bits to be communicated to the reader in the driving signal.

Carroll et al. does not disclose the limitation shown in boldface. Carroll et al. discloses the use of a resonating circuit which is tuned to the frequency of the interrogating signal. Carroll et al., col. 12, lines 1-19. Nothing is said about maintaining the resonating circuit in resonance.

Carroll et al. does not describe each and every element of claim 73 and therefore did not anticipate applicants' claim-73 invention.

Claim 74

Claim 74 reads as follows:

74. A method for responding to the establishment of an alternating magnetic field by a reader, ***[1] the reader embedding a bit-timing clock signal in the alternating magnetic field*** *and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

[3] performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field". Please see the discussion under the ***Claim 70*** heading.

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". There is no bit-timing clock signal available to Carroll et al.'s transponder 40 (see discussion under the ***Claim 70*** heading), and consequently, there is no way for transponder 40 to generate a bit-timing clock signal that is synchronized to an embedded bit-timing clock signal. Note that the only clock signal available to Carroll et al.'s "divide-by-64" timing control 60 (Fig. 3), which supplies all the timing signals for transponder 40, is the incoming FSK modulated data signal. Carroll et al., col. 12, lines 20-25. The "divide-by-64" timing control 60 is nothing more than a digital counter. Carroll et al., col. 12, lines 26-34. Nothing is said about generating a bit-timing clock signal and synchronizing it to an embedded bit-timing signal.

Limitation [3]

There is nothing in Carroll et al. that is even suggestive of Limitation [3].

Limitation [4]

Carroll et al. does not disclose "weighted integrations" and obviously does not disclose the use of weighted integrations in identifying the bit being transmitted.

Carroll et al. does not describe each and every element of claim 74 and therefore did not anticipate applicants' claim-74 invention.

Claim 75

Claim 75 reads as follows:

*75. A method for responding to the establishment of an alternating magnetic field by a reader, **[1] a bit-timing signal being embedded in the alternating magnetic field by the reader**, the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

[3] modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field". Please see the discussion under the ***Claim 70*** heading.

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". Please see the discussion under the ***Claim 74*** heading.

Limitation [3]

Carroll et al. does not disclose the transmission of bits by Carroll et al.'s transponder 40 to controller 10 wherein the start of each transmitted bit is governed by a bit-timing clock signal

that originates in controller 10. The specified bit-timing clock signal is simply not available in transponder 40 (see Limitations [1] and [2]).

Carroll et al. does not describe each and every element of claim 75 and therefore did not anticipate applicants' claim-75 invention.

Claim 76

Claim 76 reads as follows:

76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated by the responder;

the method performed by the responder comprising the steps:

[2] extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator;

generating an alternating magnetic field;

[4] embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

Carroll et al. does not disclose any of Limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field". Please see the discussion under the ***Claim 70*** heading.

Limitation [2]

Carroll et al. does not disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator". The only signal extracted by Carroll et al.'s transponder 40 is the incoming FSK modulated signal from controller 10 (col. 12, lines 20-25), the FSK modulated signal being obtained by shifting the frequency of the signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a data pulse. Carroll et al., col. 7, lines 16-29.

Extracting the data from an FSK modulated signal is NOT the same as extracting a bit-timing clock signal.

Limitation [3]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator". Please see discussion under the ***Claim 74, Limitation [2]*** headings.

Limitation [4]

Carroll et al. does not disclose the transmission of bits by transponder 40 to controller 10 wherein the start of each transmitted bit is governed by a bit-timing clock signal that originates in controller 10. Please see the discussion under the ***Claim 75, Limitation [3]*** headings.

Carroll et al. does not describe each and every element of claim 76 and therefore did not anticipate applicants' claim-76 invention.

Claim 77

Claim 77 reads as follows:

77. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field;

the method performed by the responder comprising the steps:

[2] extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of Limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field". Please see the discussion under the ***Claim 70*** heading.

Limitation [2]

Carroll et al. does not disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator". Please see the discussion under the ***Claim 76, Limitation [2]*** headings.

Limitation [3]

There is nothing in Carroll et al. that is even suggestive of Limitation [3].

Limitation [4]

Carroll et al. does not disclose "weighted integrations" and obviously does not disclose the use of weighted integrations in identifying the bit being transmitted.

Carroll et al. does not describe each and every element of claim 77 and therefore did not anticipate applicants' claim-77 invention.

Claim 78

Claim 78 reads as follows:

78. An apparatus for practicing the method of claim 73.

Carroll et al. did not anticipate claim 73 and consequently did not anticipate claim 78 which depends from claim 73.

Claim 79

Claim 79 reads as follows:

79. An apparatus for practicing the method of claim 76.

Carroll et al. did not anticipate claim 76 and consequently did not anticipate claim 79 which depends from claim 76.

Claim 80

Claim 80 reads as follows:

80. An apparatus for practicing the method of claim 77.

Carroll et al. did not anticipate claim 77 and consequently did not anticipate claim 80 which depends from claim 77.

35 U.S.C. §103(a) REJECTIONS (In View of Chatelot and Kurusu)

Claim 1

Claim 1 reads as follows:

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

a coil;

at least one capacitor;

[1] a means for coupling the capacitor(s) to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

[2] a means for extracting the data communicated by the tag from a coupling-means signal.

Limitation [1]

As the examiner points out, Chatelot does not disclose Limitation [1]. Kurusu shows a

receiving antenna 11 that feeds a received signal through a filter 13 to amplifier 12 which outputs an amplified version of the received signal. Amplifier 12 includes input coupling transformer 17, capacitor 22 connected across the input winding of transformer 17, and RC circuit 21 which (together with RC circuit 23) provides proper biasing of transistor 16. Kurusu, Fig. 1.

The examiner argues that Chatelot's capacitors 19 are analogous to Kurusu's capacitor in RC circuit 21 and Chatelot's transmission coil 14 is analogous to Kurusu's receiving antenna 11. *See* Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention.

The examiner's conclusion is questionable when one considers what is necessary to establish a *prima facie* case of obviousness:

> **"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP § 2142.**

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in

an overvoltage protecting arrangement for an RF amplifier used to amplify received signals. The use of a transformer for coupling received signals into an amplifier (Kurusu) has little or nothing to do with coupling a driving signal to a coil (Chatelot).

Nor would a person skilled in the art be motivated to use Kurasu's transformer for "coupling the coil to at least one other means" as specified in claim 1.

With respect to teaching or suggesting Limitation [1], there is no teaching of "a means for driving the coil through the capacitor(s) with a driving signal" wherein the "means for coupling the capacitor(s) to the coil . . . [is] a transformer". The capacitor in RC circuit 21 (Kurusu, Fig. 1) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways of driving signals to coil 13. Thus, Kurusu provides no information as to how to incorporate Kurusu's transformer in Chatelot's invention. Does the person skilled in the art simply insert Kurusu's transformer 17 between Chatelot's capacitors 19 and coil 13 as applicants specify in claim 1? Or does the person skilled in the art place Kurusu's transformer 17 on the other side of Chatelot's capacitors 19? There is no teaching as to what to do.

Limitation [2]

Limitation [2] specifies that data is to be extracted from a coupling means signal which originates in a transformer located between capacitor(s) through which the driving signal passes and the coil.

Chatelot does not disclose this limitation since Chatelot does not disclose a transformer located between capacitor(s) 19 and coil 13. Chatelot extracts data from signals picked up from the capacitor terminals NOT connected to the coil (Chatelot, Fig. 3), and consequently, even if Chatelot had disclosed a transformer located between capacitor(s) 19 and coil 13, he would not have disclosed Limitation [2].

There is no teaching in Chatelot and/or Kurusu that would cause a person skilled in the art to incorporate the transformer disclosed by Kurusu in Chatelot's invention at a location between capacitor(s) 19 and coil 13. Nor would there be motivation for a person skilled in the art to make such a modification even if there were such a teaching. For a discussion of these issues, please see above under the heading ***Limitation [1].***

Chatelot and Kurusu in combination fail to teach all of the claim limitations of claim 1. Even if the combination did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination.

The examiner has not established the *prima facie* obviousness of claim 1.

Claim 3

Claim 3 reads as follows:

3. The reader of claim 1 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the second winding.

Neither Chatelot nor Kurusu show the configuration specified in claim 3. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-3 limitations.

The examiner has not established the *prima facie* obviousness of claim 3.

Claim 41

Claim 41 reads as follows:

41. A tag for use with a reader, the tag comprising:

a coil;

a capacitor;

a means for driving the coil;

[1] a means for coupling the capacitor and the driver to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

[2] a means for extracting the data communicated by the reader from a coupling-means signal;

[3] a means for extracting power from the coupling-means signal to operate the tag.

Limitation [1]

Chatelot does not teach a configuration for data carrier 12 (analogous to applicants' tag) and consequently there is no disclosure of Limitation [1]

Limitation [2]

Chatelot does not teach the coupling means (i.e. transformer) of Limitation [1], and consequently, there can be no teaching of "a means for extracting the data communicated by the reader from a coupling-means signal."

Limitation [3]

Chatelot does not teach the coupling means (i.e. transformer) of Limitation [1], and consequently, there can be no teaching of "a means for extracting power from the coupling-means signal to operate the tag."

Limitations [1], [2], and [3] of claim 41 are not disclosed by the references, and the *prima facie* obviousness of claim 41 has not been established.

Claim 43

Claim 43 reads as follows:

43. The tag of claim 41 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor and the driving means being connected to the first winding, the coil, the data-extraction means, and the power-extraction means being connected to the second winding.

Chatelot does not disclose a configuration for data carrier 12 (analogous to applicants' tag), and consequently, Chatelot does not disclose the claim-43 limitations.

The examiner has not established the *prima facie* obviousness of claim 43.

35 U.S.C. §103(a) REJECTIONS (In View of Chatelot and Ogita et al.)

Claim 1

Claim 1 reads as follows:

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

a coil;

at least one capacitor;

[1] a means for coupling the capacitor(s) to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

[2] a means for extracting the data communicated by the tag from a coupling-means signal.

Limitation [1]

As the examiner points out, Chatelot does not disclose Limitation [1]. Ogita et al. shows a receiving antenna 21 that feeds a received signal through transformer 31 to amplifier 37 which outputs an amplified version of the received signal. Ogita et al., Fig. 8. The examiner argues that Ogita et al.'s capacitor 34 is analogous to Chatelot's capacitors 19, and Ogita et al.'s receiving antenna 21 is analogous to Chatelot's transmission coil 13. *See* Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Ogita et al.'s transformer 31 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention.

The examiner's conclusion is questionable when one considers what is necessary to establish a *prima facie* case of obviousness:

> **"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP § 2142.**

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in Ogita et al.'s impedance matching a receiving antenna to an amplifier for Chatelot's direct connections of capacitors 19 to coil 13. The use of a transformer for impedance matching in a receiving circuit (Ogita et al.) has little or nothing to do with coupling a driving signal to a coil for the purpose of interrogating a tag (Chatelot).

Nor would a person skilled in the art be motivated to use Ogita et al.'s transformer for "coupling the coil to at least one other means" as specified in claim 1.

The examiner argues that the motivation for incorporating Ogita et al.'s transformer in Chatelot's invention is "to provide isolation between the communication antenna coil and the other circuits in the reader." However, such a modification would appear to be unnecessary since Chatelot states that with his reading-writing station "a rapid and reliable data exchange may be made with a user system such as a programmable automation or other system controlling an industrial process." Chatelot, col. 2, lines 3-6. Where is the motivation to modify (and at the same time complicate) a system that is already capable of operating satisfactorily?

With respect to teaching or suggesting all the claim limitations, there is no teaching of "a means for driving the coil through the capacitor(s) with a driving signal" wherein the "means for coupling the capacitor(s) to the coil . . . [is] a transformer". Capacitor 34 (Ogita et al., Fig. 8) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways for driving signals to coil 13. Thus, Ogita et al. provides no information as to how to incorporate Ogita et al.'s transformer in Chatelot's invention. Does the person skilled in the art

simply insert Ogita et al.'s transformer 31 between Chatelot's capacitors 19 and coil 13 as applicants specify in claim 1? Or does the person skilled in the art place Ogita et al.'s transformer 31 on the other side of Chatelot's capacitors 19? There is no teaching as to what to do.

Chatelot and Ogita et al. in combination fail to teach all of the claim limitations of claim 1. Even if the references did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination.

The examiner has not established the *prima facie* obviousness of claim 1.

Claim 2

Claim 2 reads as follows:

2. The reader of claim 1 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the first winding.

Neither Chatelot nor Ogita et al. show the configuration specified in claim 2. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-2 limitations.

The examiner has not established the *prima facie* obviousness of claim 2.

Claim 4

Claim 4 reads as follows:

4. The reader of claim 1 wherein the coupling means is a transformer having a first winding, a second winding, and a third winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the third winding.

Neither Chatelot nor Ogita et al. show the configuration specified in claim 4. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-4 limitations.

The examiner has not established the *prima facie* obviousness of claim 4.

Claim 41

Claim 41 reads as follows:

41. A tag for use with a reader, the tag comprising:

a coil;

a capacitor;

a means for driving the coil;

[1] a means for coupling the capacitor and the driver to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

[2] a means for extracting the data communicated by the reader from a coupling-means signal;

[3] a means for extracting power from the coupling-means signal to operate the tag.

Limitation [1]

Chatelot does not teach a configuration for data carrier 12 (analogous to applicants' tag) and consequently there is no disclosure of Limitation [1]

Limitation [2]

Chatelot does not teach the coupling means (i.e. transformer) of Limitation [1], and consequently, there can be no teaching of "a means for extracting the data communicated by the reader from a coupling-means signal."

Limitation [3]

Chatelot does not teach the coupling means (i.e. transformer) of Limitation [1], and consequently, there can be no teaching of "a means for extracting power from the coupling-means signal to operate the tag."

Limitations [1], [2], and [3] of claim 41 are not disclosed by the references, and the *prima facie* obviousness of claim 41 has not been established.

Claim 42

Claim 42 reads as follows:

42. The tag of claim 41 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor, the driving means, the data-extraction means, and the power-extraction means being connected to the first winding, the coil being connected to the second winding.

Chatelot does not disclose a configuration for data carrier 12 (analogous to applicants' tag), and consequently, Chatelot does not disclose the claim-42 limitations.

The examiner has not established the *prima facie* obviousness of claim 42.

Claim 44

Claim 44 reads as follows:

44. The tag of claim 41 wherein the coupling means is a transformer having a first winding, a second winding, and a third winding, the capacitor and the driving means being connected to the first winding, the data-extraction means and the power-extraction means being connected to the second winding, and the coil being connected to the third winding.

Chatelot does not disclose a configuration for data carrier 12 (analogous to applicants' tag), and consequently, Chatelot does not disclose the claim-44 limitations.

The examiner has not established the *prima facie* obviousness of claim 44.

Claim 45

Claim 45 reads as follows:

45. The tag of claim 41 wherein the coupling means is a transformer having a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the driving means being connected to the first winding, the data-extraction means being connected to the second winding, the power-extraction means being connected to the third winding, and the coil being connected to the fourth winding.

Chatelot does not disclose a configuration for data carrier 12 (analogous to applicants' tag), and consequently, Chatelot does not disclose the claim-45 limitations.

The examiner has not established the *prima facie* obviousness of claim 45.

35 U.S.C. §103(a) REJECTIONS (In View of Carroll et al.)

Claim 5

Claim 5 reads as follows:

5. A reader for use with a tag, the reader comprising:

a coil;

[1] at least one capacitor;

[2] a means for coupling the capacitor(s) to the coil;

[3] a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

[4] a means for embedding a bit-timing clock signal in the driving signal;

a means for embedding a sequence of bits to be communicated to a tag in the driving signal.

Carroll et al. does not disclose any of the limitations shown in boldface above.

Limitations [1], [2], and [3]

Carroll et al. utilizes microprocessor 12 to directly drive coil 18 by means of coil drive circuit 16. No capacitor is involved in the process. Carroll et al., col. 6, lines 7-9. Thus, Carroll et al. does not disclose limitations [1], [2], and [3].

Limitation [4]

Carroll et al. does not disclose Limitation [4]. The figure cited by the examiner (Carroll et al., Fig. 4b) refers to the situation when transponder 40 has responded to an interrogation by controller 10 and controller 10 has bit-synchronized to transponder 40's transmission (Carroll et al., col. 14, line 60 - col. 15, line 67). Then (with reference to Fig. 4B), controller 10 "either

reads from, or writes to, the non-volatile memory 48 of the transponder 40 by sending a command word 112. The command word 112 is transmitted in bit for bit synchronization with the configuration word 100 or any data being sent from the transponder 40 to the controller 10." Carroll et al., col. 16, lines 1-10. Synchronization block 114 are logic level zero bits and is NOT a bit-timing clock signal. Carroll et al., col. 16, lines 7-10.

Carroll et al.'s controller 10 only transmits FSK modulated data signals. Carroll et al., col. 6, lines 7-9; col. 7, lines 5-12. Carroll et al. does not embed a bit-timing clock signal in the alternating magnetic field because FSK detector 64 in transponder 40 does not require a bit-timing signal. *See* references cited, Carroll et al., col. 12, lines 36-46.

> **"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."** MPEP § 2142.

Carroll et al. does not "teach or suggest all the claim limitations" of claim 5 and *prima facie* obviousness of claim 5 has not been established.

Claim 6

Claim 6 reads as follows:

6. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal. Controller 10 embeds a sequence of bits in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not a teaching of the claim-6 limitation.

The examiner seems to argue that because Carroll et al.'s transponder 40 responds to controller 10's interrogation with a PSK signal, a person skilled in the art would be motivated to change controller 10's means for communicating data to PSK. However, there is no suggestion in Carroll et al. or in the knowledge generally available to one of ordinary skill in the art to make such a change. Carroll et al. chose the simple means of varying the frequency of the driving signal for communicating data from controller 10 to transponder 40 because the detection of frequency changes is particularly simple and does not require a bit-timing clock signal to be available in transponder 40 thereby resulting in a less-complicated and less-costly transponder.

There is no motivation for changing controller 10's method of transmitting data to transponder 40, and consequently, *prima facie* obviousness of applicants' claim-6 invention has not been established.

Claim 7

Claim 7 reads as follows:

7. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 7.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the limitation of claim 7, and consequently, *prima facie* obviousness of claim 7 has not been established.

Claim 8

Claim 8 reads as follows:

8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 8.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the limitation of claim 8, and consequently, *prima facie* obviousness of claim 8 has not been established.

Claim 9

Claim 9 reads as follows:

9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 9.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the limitation of claim 9, and consequently, *prima facie* obviousness of claim 9 has not been established.

Claim 10

Claim 10 reads as follows:

10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 10.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as "causing the phase of the driving signal to have a

first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted" .

Carroll et al. does not teach the limitation of claim 10, and consequently, *prima facie* obviousness of claim 10 has not been established.

Claim 11

Claim 11 reads as follows:

11. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 11.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 11, and consequently, *prima facie* obviousness of claim 11 has not been established.

Claim 12

Claim 12 reads as follows:

12. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 12.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 12, and consequently, *prima facie* obviousness of claim 12 has not been established.

Claim 13

Claim 13 reads as follows:

13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 13.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 13, and consequently, *prima facie* obviousness of claim 13 has not been established.

Claim 25

Claim 25 reads as follows:

25. A reader for use with a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated, the reader comprising:

a means for receiving the tag signal;

a means for measuring the period of each cycle of the signal received from the tag during a bit period.

Carroll et al. does not teach the limitation shown in boldface, and consequently, *prima facie* obviousness of claim 25 has not been established.

Claim 26

Claim 26 reads as follows:

26. The reader of claim 25 further comprising:

a means for identifying the bit transmitted by the tag from the measurements of the period of each cycle of the signal received from the tag during a bit period.

Carroll et al. does not teach the limitation of claim 26, and consequently, *prima facie* obviousness of claim 26 has not been established.

Claim 27

Claim 27 reads as follows:

27. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

Carroll et al. does not teach the limitations of claim 27, and consequently, *prima facie* obviousness of claim 27 has not been established.

Claim 28

Claim 28 reads as follows:

28. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

Carroll et al. does not teach the limitations of claim 28, and consequently, *prima facie* obviousness of claim 28 has not been established.

Claim 29

Claim 29 reads as follows:

29. The reader of claim 25 further comprising:

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change greater than a predetermined value in the period of a cycle from one cycle to the next cycle.

Carroll et al. does not teach the limitation of claim 29, and consequently, *prima facie* obviousness of claim 29 has not been established.

Claim 30

Claim 30 reads as follows:

30. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between

the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

Carroll et al. does not teach the limitations of claim 30, and consequently, *prima facie* obviousness of claim 30 has not been established.

Claim 31

Claim 31 reads as follows:

31. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

Carroll et al. does not teach the limitations of claim 31, and consequently, *prima facie* obviousness of claim 31 has not been established.

Claim 47

Claim 47 reads as follows:

47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit;

[1] a means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals;

[2] a means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal.

Limitation [1]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40. Consequently, there is no bit-timing clock signal originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock.

Carroll et al. does not teach Limitation [1].

Limitation [2]

Carroll et al.'s transponder 40 has no information available from controller 10 as to the beginning and ending of a bit period and therefore does not teach the use of this information in identifying the bit being transmitted during the bit period.

Carroll et al. does not teach Limitation [2].

Carroll et al. does not teach the limitations of claim 47, and consequently, *prima facie* obviousness of claim 47 has not been established.

Claim 48

Claim 48 reads as follows:

48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-48 limitations.

Carroll et al. does not teach the limitations of claim 48, and consequently, *prima facie* obviousness of claim 48 has not been established.

Claim 49

Claim 49 reads as follows:

49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

The examiner argues that "amplitude shift keying is a common alternative to phase shift keying or frequency shift keying, and to have substituted this type of modulation scheme for that used in Carroll would not have involved an unobvious step." 04/04/03 Office Action, p. 9. There is no mention of amplitude shift keying in claim 49 or in claim 47 from which claim 49 depends. It would appear that the examiner's comment is irrelevant insofar as the patentability of applicants' claim-49 invention is concerned.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-49 limitations.

Carroll et al. does not teach the limitations of claim 49, and consequently, *prima facie* obviousness of claim 49 has not been established.

Claim 50

Claim 50 reads as follows:

50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-50 limitations.

Carroll et al. does not teach the limitations of claim 50, and consequently, *prima facie* obviousness of claim 50 has not been established.

Claim 51

Claim 51 reads as follows:

51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

Carroll et al. does not teach the limitations of claim 51, and consequently, *prima facie* obviousness of claim 51 has not been established.

Claim 52

Claim 52 reads as follows:

52. The reader of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal

parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

Carroll et al. does not teach the limitations of claim 52, and consequently, *prima facie* obviousness of claim 52 has not been established.

Claim 53

Claim 53 reads as follows:

53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal;

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration;

a means for translating the first and second integrations into a bit value.

Carroll et al. does not teach the limitations of claim 53, and consequently, *prima facie* obviousness of claim 53 has not been established.

Claim 54

Claim 54 reads as follows:

54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transition in the coupling-means signal from one bit to the next;

a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously.

Carroll et al. does not teach the limitations of claim 54, and consequently, *prima facie* obviousness of claim 54 has not been established.

Claim 55

Claim 55 reads as follows:

55. The tag of claim 47 wherein the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second signal, the means for generating a bit-timing clock signal that indicates the start of each bit period comprising:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal;

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously.

Carroll et al. does not teach the limitations of claim 55, and consequently, *prima facie* obviousness of claim 55 has not been established.

Claim 56

Claim 56 reads as follows:

56. A tag for use with a reader, the reader transmitting a bit-timing clock signal to the tag, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil;

a means for driving the coil with a driving signal;

a means for generating the driving signal;

[1] a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;

[2] a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

Limitation [1]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40. *See* discussion under ***Claim 5, Limitation [4]*** headings. Consequently, there is no bit-timing clock signal originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock.

Carroll et al. does not teach Limitation [1].

Limitation [2]

Carroll et al.'s transponder 40 does not receive a bit-timing clock signal from controller 10 and consequently has no means for generating a bit-timing clock signal synchronized to a controller 10 bit-timing clock signal and no means for embedding a sequence of bits to be communicated to controller 10 in the driving signal wherein the start of each bit is controlled by the bit-timing clock signal.

Carroll et al. does not teach Limitation [2].

Carroll et al. does not teach Limitations [1] and [2], and consequently, *prima facie* obviousness of claim 56 has not been established.

Claim 57

Claim 57 reads as follows:

57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

Carroll et al. teach the use of Manchester coded PSK in transmitting data from transponder 40 (analogous to applicants' tag) to controller 10. Carroll et al., col. 20, lines 33-35. Manchester-coded PSK results in the driving signal having (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) a second phase during the first half of a bit period and a first phase during the second half of a bit period when a "1" is transmitted. Manchester-coded PSK is not a teaching of applicants' claim-57 limitation.

Manchester-coded PSK has some very desirable properties, and a person skilled in the art would not be motivated by knowledge generally available to one of ordinary skill in the art to change Carroll et al.'s modulation technique to the one specified in applicants' claim 57.

Carroll et al. does not teach the claim-57 limitation, and consequently, *prima facie* obviousness of claim 57 has not been established.

Claim 58

Claim 58 reads as follows:

58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 58.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the limitation of claim 58, and consequently, *prima facie* obviousness of claim 58 has not been established.

Claim 59

Claim 59 reads as follows:

59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 59.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the limitation of claim 59, and consequently, *prima facie* obviousness of claim 59 has not been established.

Claim 60

Claim 60 reads as follows:

60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 60.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the limitation of claim 60, and consequently, *prima facie* obviousness of claim 60 has not been established.

Claim 62

Claim 62 reads as follows:

62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 62.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first

frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 62, and consequently, *prima facie* obviousness of claim 62 has not been established.

Claim 63

Claim 63 reads as follows:

63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 63.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 63, and consequently, *prima facie* obviousness of claim 63 has not been established.

Claim 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 64, and consequently, *prima facie* obviousness of claim 64 has not been established.

Claim 69

Claim 69 reads as follows:

69. The tag of claim 56 wherein the reader transmits the bit-timing clock signal to the tag by communicating a sequence of alternating "0" and "1" bits, a "0" bit being communicated by modulating the amplitude of the driving signal with a first periodic signal, a "1" bit being communicated by modulating the amplitude of the alternating field with a second periodic signal, ***[claim-56 limitation] the means for generating the clock signal that is synchronized to the bit-timing signal transmitted by the reader to the tag*** *comprising:*

[1] a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

[2] a means for obtaining the amplitude of a coupling-means signal as a function of time;

[3] a means for recognizing the transitions in the coupling-means signal amplitude at the time interfaces of the first and second periodic signals;

[4] a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal amplitude occur simultaneously.

As the claim states, the means shown in boldface in the preamble, a claim-56 limitation, is comprised of Limitations [1], [2], [3], and [4]. None of these limitations are taught by Carroll et al.

Carroll et al. does not teach the limitations of claim 69, and consequently, *prima facie* obviousness of claim 69 has not been established.

35 U.S.C. §103(a) REJECTIONS (In View of Waraksa et al. & Batz et al.)

Claim 34

Claim 34 reads as follows:

34. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

a means for determining whether the oldest S bits in memory is a sync sequence;

[1] a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

[2] a control means for causing the determining means and the replacing means to operate alternately after the memory is filled with received bits.

Neither Waraksa et al. nor Batz et al. teach Limitations [1] and [2].

The tag of applicants' invention, after it is interrogated by a reader, continually transmits a repeated message consisting of S sync bits, T tag data bits, and T error-detecting bits. The reader, by the time it is ready to extract data from the tag's transmission, may begin obtaining data in the middle of a message. In order to detect errors and extract the tag data from the message, it must first identify the sync bits. It does this by storing the bits as they arrive and continually examining the oldest S bits to determine whether they correspond to the sync sequence. If they do not, the oldest bit is discarded and the "new" oldest S bits is examined. This process is repeated until the sync bits are discovered.

Neither of the references cited by the examiner teach this process. The examiner argues that Batz et al. discloses the claim-34 limitations and cites col. 14, lines 42+. But the first line of the cited passage reveals that there is no uncertainty in the Batz et al. interrogation as to the identity of the sync bits: "The sync word shift register 225 receives and decodes the first eight

bits which correspond to the sync word portion of the incoming interrogate signal." Batz et al., col. 14, lines 43-45. There is no uncertainty in the Batz et al. system as to which bits in the received interrogation correspond to the sync word. The sync word consists of the first eight bits received. The primary concern in the Batz et al. system is that a responder only responds to an interrogation having a valid sync word.

Limitation [1]

Batz et al. does not disclose "replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits". Batz et al. simply wait until the first eight bits of an interrogation message has been received and then determines whether this eight-bit "received" sync word corresponds to a stored sync word. If it is not, the interrogation cycle ends. Batz et al., col. 4, lines 35-38.

Limitation [2]

Batz et al. does not disclose "causing the determining means and the replacing means to operate alternately after the memory is filled with received bits". Batz et al.'s "determining means" which determines whether the oldest S bits in memory is a sync sequence operates only once immediately after the first 8 bits of the interrogation message is received. Batz et al., col.4, lines 6-53.

The references cited by the examiner do not teach the limitations of claim 34, and consequently, *prima facie* obviousness of claim 34 has not been established.

Claim 35

Claim 35 reads as follows:

35. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

[1] a first means for determining whether the newest S bits in memory is a sync sequence;

[2] a second means for determining whether the oldest S bits in memory is a sync sequence;

[3] a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

[4] a control means for causing the first determining means and the replacing means to operate alternately until a sync sequence is detected, the control means causing the second determining means and the replacing means to operate alternately if a detected sync sequence is determined to be a false-sync sequence.

Neither Waraksa et al. nor Batz et al. teach the limitations shown in boldface.

The tag of applicants' invention, after it is interrogated by a reader, continually transmits a repeated message consisting of S sync bits, T tag data bits, and T error-detecting bits. The reader, by the time it is ready to extract data from the tag's transmission, may begin obtaining data in the middle of a message. In order to detect errors and extract the tag data from the message, it must first identify the sync bits. It does this by storing the bits as they arrive and continually examining the oldest S bits to determine whether they correspond to the sync sequence. If they do not, the oldest bit is discarded and the "new" oldest S bits is examined. This process is repeated until the sync bits are discovered.

Neither of the references cited by the examiner teach this process. The examiner argues that Batz et al. discloses the claim-35 limitations and cites col. 14, lines 42+. But the first line of the cited passage reveals that there is no uncertainty in the Batz et al. interrogation as to the

identity of the sync bits: "The sync word shift register 225 receives and decodes the first eight bits which correspond to the sync word portion of the incoming interrogate signal." Batz et al., col. 14, lines 43-45. There is no uncertainty in the Batz et al. system as to which bits in the received interrogation correspond to the sync word. The sync word consists of the first eight bits received. The primary concern in the Batz et al. system is that a responder only responds to an interrogation having a valid sync word.

Limitations [1] and [2]

Batz et al. does not envision a situation where the identification of a sync sequence involves both a determination as to whether the newest S bits is a sync sequence and a determination as to whether the oldest S bits in memory is a sync sequence. Batz et al. is only concerned with the first-arriving eight bits. Batz et al., col. 4, lines 35-37.

Limitation [3]

Batz et al. does not disclose "replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits". Batz et al. simply wait until the first eight bits of an interrogation message has been received and then determines whether this eight-bit "received" sync word corresponds to a stored sync word. If it is not, the interrogation cycle ends. Batz et al., col. 4, lines 35-38.

Limitation [4]

There is nothing in Batz et al. that teaches this limitation.

The references cited by the examiner do not teach the limitations of claim 35, and consequently, *prima facie* obviousness of claim 35 has not been established.

35 U.S.C. §103(a) REJECTIONS (In View of Carroll et al. & McFarlane)

Claim 14

Claim 14 reads as follows:

14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. Thus, McFarlane does not teach the limitation of claim 15.

Carroll et al. utilize a simple FSK technique for communicating commands from controller 10 to transponder 40 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by a simple circuit consisting of an oscillator, an up/down counter, and logic circuits. Carroll et al., col. 18, lines 44-57. McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two

filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

The examiner argues that the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s FSK circuitry would result in a reader with the properties specified by the limitations of claim 14. The motivation for a person skilled in art, argues the examiner, is to increase the bandwidth of the system.

However, there is no suggestion in Carroll et al. that additional communication capacity from controller 10 to transponder 40 is needed. And the additional complexity of both the controller and the transponder required to obtain the additional communication capacity would certainly be undesirable.

Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-14 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. The examiner has not established *prima facie* obviousness of applicants' claim-14 invention.

Claim 15

Claim 15 reads as follows:

15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first

frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 15.

Neither Carroll et al. nor McFarlane teach the limitation of claim 15 and *prima facie* obviousness of claim 15 has not been established.

Claim 16

Claim 16 reads as follows:

16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-16 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this

modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 16.

Neither Carroll et al. nor McFarlane teach the limitation of claim 16 and *prima facie* obviousness of claim 16 has not been established.

Claim 17

Claim 17 reads as follows:

17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-17 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 17.

Neither Carroll et al. nor McFarlane teach the limitation of claim 17 and *prima facie* obviousness of claim 17 has not been established.

Claim 61

Claim 61 reads as follows:

61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane disclose a modulation technique wherein the PHASE of the driving signal has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. This is NOT the same as a modulation technique wherein the DRIVING SIGNAL has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane teach the limitation of claim 61 and *prima facie* obviousness of claim 61 has not been established.

Claim 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-64 limitation has to do with applying FSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 64.

Neither Carroll et al. nor McFarlane teach the limitation of claim 64 and *prima facie* obviousness of claim 64 has not been established.

Claim 65

Claim 65 reads as follows:

65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second

frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. Thus, McFarlane does not teach the limitation of claim 15.

Carroll et al. utilize a simple PSK technique for communicating data from transponder 40 to controller 10 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by the microcomputer chip. Carroll et al., col. 7, lines 12-16. McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

The examiner argues that the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s PSK circuitry would result in a transponder with the properties specified by the limitations of claim 65. The motivation for a person skilled in art, argues the examiner, is to increase the bandwidth of the system.

However, there is no suggestion in Carroll et al. that additional communication capacity from transponder 40 to controller 10 is needed. And the additional complexity of both the

controller and the transponder required to obtain the additional communication capacity would certainly be undesirable.

Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-65 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique. The examiner has not established *prima facie* obviousness of applicants' claim-65 invention.

Claim 66

Claim 66 reads as follows:

66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 66.

Neither Carroll et al. nor McFarlane teach the limitation of claim 66 and *prima facie* obviousness of claim 66 has not been established.

Claim 67

Claim 67 reads as follows:

67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-16 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 67.

Neither Carroll et al. nor McFarlane teach the limitation of claim 67 and *prima facie* obviousness of claim 67 has not been established.

Claim 68

Claim 68 reads as follows:

68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-17 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 68.

Neither Carroll et al. nor McFarlane teach the limitation of claim 68 and *prima facie* obviousness of claim 68 has not been established.

DOUBLE-PATENTING REJECTIONS BASED ON BEIGEL et al. (P.N. 6,472,975)

Claims 1-31, 36-80

The present application is a division of application 08/262,157, now U.S. Patent No. 6,472,975. Double patenting rejections are prohibited under 35 U.S.C. 121. Please see Manual of Patent Examining Procedure § 804.01, a copy of which is included as Attachment III. None of the exceptions (A) through (F) apply.

Please note in particular the last paragraph of the attachment which states that 35 U.S.C. 121 does not apply when the identical invention is claimed in both the patent and the pending

application. However, the examiner correctly observes in his office action that "the conflicting claims are not identical."

Applicants request the withdrawal of the double-patenting rejections based on U.S. Patent No. 6,472,975.

DOUBLE-PATENTING REJECTIONS BASED ON BEIGEL et al. (P.N. 5,235,326)

Claims 36-40, 70-80

Claim 16 of Beigel et al. '326 includes the following three limitations:

a means for storing mode control data;

a means for obtaining a measure of the time-dependent absorption of power from said magnetic field by an electronic identification tag, said power absorption measure representing information being communicated by said tag;

a means for extracting said information from said power absorption measure, said information extracting means operating in at least one of a plurality of information extracting modes, each of said information extracting modes defining a specific functional relationship between said information and said time-dependent absorption of power by said tag, said information extracting modes being characterized by said mode control data, the specification of the information extracting mode in said mode control data permitting the extraction of information from said time-dependent absorption of power by said tag.

There are no limitations like the above in any of the claims of the present application. As the Manual of Patent Examining Procedure states, "In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is—does any claim in the application define an invention that is merely an obvious variation of an invention claimed in the

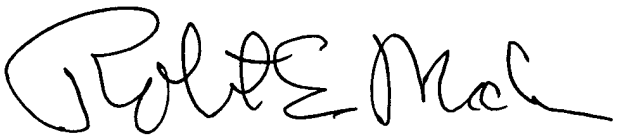
patent?" MPEP § 804 II B 1. When none of the claims of the application contain any of three limitations of the patent, the answer to this question must be no.

There is no basis for the double-patenting rejections of the above-referenced claims.

* * * * *

Claims 1-80 appear to be in condition for allowance and such action is respectfully requested.

Respectfully submitted,



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